90

Electrical / IV / CBGS
ADIC

10.6.14

QP Code :**NP-19827**

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No. **1** is **compulsory**.
(2) Solve any **three** from remaining questions.
(3) Assume suitable data wherever **necessary.**

1. (a) Draw the block diagram of op-amp and explain function of each block. **4**
(b) Define following terms w.r.t. op-amp **4**
(i) CMRR
(ii) Slew rate.
(c) Explain terms line regulation, load regulation and dropout voltage for linear IC regulators. **4**
(d) Convert **4**
(i) $(8A9{\cdot}B4)_{16}$ to Binary
(ii) $(615{\cdot}25)_{8}$ to Hexadecimal.
(e) (i) List application of Flip-flops **4**
(ii) What are basic types of shift registors in terms of data movement.

2. (a) Explain with waveform working of a positive clipper circuit. **4**
(b) Explain working of Schmitt triger along with waveforms. Also derive the equations for trigger point voltages. **8**
(c) (i) Draw circuit diagram for op-amp as inverting summing amplifier and derive equation for output voltage. **8**
(ii) Draw and explain operation of half wave precision rectifier.

3. (a) Explain voltage to current converter with grounded load. **4**
(b) Design a first order low pass filter for cut-off frequency of 2 KHz and pass band gain of 2. Draw circuit diagram and plot the frequency response. **8**
(c) Explain IC 555 as monostable multivibrator. **8**

4. (a) Op-amp is configured as integrator. Draw output waveforms when input to the circuit is– **4**
(i) Square wave
(ii) Sine wave
(b) Give the specifications of digital IC. **4**
(c) Explain dual slope analog to digital converter. **4**
(d) Design two bit magnitude comparator and implimernt using logic gates. **8**

5. (a) Simplify using Boolean laws– **4**

$$AB + \overline{AC} + A\,\overline{B}\,C \quad (AB + C)$$

(b) Minimize the given function using k-maps and realize using universal gates. **8**
$f(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$
(c) (i) Explain in short hazads in combinational circuits. **8**
(ii) Implement using 8 : 1 multiplexer
$f(A, B, C, D) = 0, 2, 3, 6, 8, 9, 12, 14)$

6. (a) Write note on interfacing between TTL and CMOS logic families. **4**
(b) Convert SR flipflop to JK flip-flop. **4**
(c) State differences between synchronous and asynchronous counters. **4**
(d) Design a mod-5 synchronous counter using JK flip-flop and implement it. Draw timing diagram. **8**

Con. 13335-14.